RL4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/558,542	04/26/2000	Sri Ram Gorti	105178	9596

7590 08/26/2003

Oliff & Berridge PLC
PO Box 19928
Alexandria, VA 22320

EXAMINER
NAHAR, QAMRUN

ART UNIT	PAPER NUMBER
2124	6

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

P22

Office Action Summary	Application No. 09/558,542	Applicant(s) GORTI ET AL.	
	Examiner Qamrun Nahar	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed on 7/3/03.

2. Claims 1-20 are pending.

3. Claims 1-20 stand finally rejected under 35 U.S.C. 102(b) as being anticipated by Benson (U.S. 5,301,325).

Response to Amendment

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Benson (U.S. 5,301,325).

Per Claim 1:

The Benson patent discloses:

- a code translation device that translates a source code of a source processor into a target code of a target processor ("In accordance with one embodiment of the invention, a code translator is constructed in a manner similar to a compiler, and may indeed be implemented as part of a compiler. The code translator accepts as an input the assembly code or source code

which is to be translated, in a manner similar to the front end of any compiler. The input code is parsed to determine its content, with the basic building blocks of the code identified (separated) and converted into an intermediate language. The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine. This translator is particularly adapted for translating VAX assembly language into an advanced RISC architecture." in column 4, lines 3-18)

- **a memory** ("Fig. 2 is an electrical diagram of a host computer for executing the code translator program of Fig. 1" in column 7, lines 44-45 and Fig. 2, item 15, "MEMORY")

- **a controller, the controller dividing the source code into translated code blocks of the target code based on a target processor register capability** ("The code translator accepts as an input the assembly code or source code which is to be translated, in a manner similar to the front end of any compiler. The input code is parsed to determine its content, with the basic building blocks of the code identified (separated) and converted into an intermediate language. The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine. ... Another feature of interest in converting code from one architecture to another is that of register usage. ... In code generated by the compiler for register saves for an advanced 64-bit RISC architecture, only the low 32-bits of the 64-bit register can be put on the stack ... Accordingly, in one embodiment of the invention, the

compiler tracks register usage to determine which registers are destroyed by a routine, and generate routine prologue and epilogue code which performs 64-bit register saves." in column 4, lines 3-18; and column 4, lines 67-68 to column 5, lines 1-18).

Per Claim 2:

The Benson patent discloses:

- a branch detector, the branch detector identifying one or more instructions of the source code that either includes a branch, a loop return or an entry point for a branch or loop return (column 4, lines 44-61 and column 10, lines 20-30).

Per Claim 3:

The Benson patent discloses:

- wherein the controller generates one or more source code blocks based on the identified instructions, each of the source code blocks beginning immediately after an identified instruction and includes all consecutive instructions following the identified instruction up to an instruction immediately before a next identified instruction (column 10, lines 20-36 and lines 44-66).

Per Claim 4:

The Benson patent discloses:

- wherein the controller identifies source register types of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding target registers that correspond to the selected source register types as the target register capability (column 6, lines 64-68 to column 7, lines 1-7; and column 7, lines 19-30).

Per Claim 5:

The Benson patent discloses:

- further comprising a register detector, the register detector detecting a number of source registers that are used and/or updated in one or more instructions of each of the source code blocks (column 6, lines 57-68 to column 7, lines 1-7).

Per Claim 6:

The Benson patent discloses:

- wherein the controller generates one or more translated code blocks for each of the source code blocks based on a number of selected source registers detected by the register detector and the maximum numbers of corresponding target registers (column 5, lines 14-47).

Per Claim 7:

The Benson patent discloses:

- further comprising a stub generator, the stub generator generating a head stub and a tail stub for each of the translated code blocks (column 5, lines 14-18).

Per Claim 8:

The Benson patent discloses:

- wherein a head stub associated with a translated code block initializes one or more target registers used by the associated translated code block, the target registers being initialized by retrieving register values from a source register map that stores values of the source registers during execution of the translated code blocks (column 5, lines 18-43; column 6, lines 57-68 to column 7, lines 1-7; and column 7, lines 19-30).

Per Claim 9:

The Benson patent discloses:

- wherein a tail stub associated with a translated code block saves values of one or more target registers used by the associated translated code block in a source register map after execution of the translated code block (column 5, lines 18-40 and lines 45-47; column 6, lines 57-68 to column 7, lines 1-7; and column 7, lines 19-30).

Per Claim 10:

The Benson patent discloses:

- wherein the source register map includes storage space for one or more values for each source register accounting for instruction execution delays, the tail stub saves values of the target registers in one or more appropriate locations in the source register map to account for the instruction execution delays (column 7, lines 19-30; column 21, lines 42-43 to column 22, lines 1-2).

Per Claim 11:

This is a method version of the claimed device discussed above, claim 1, wherein all claim limitations also have been addressed and/or covered in cited areas as set forth above, including "identifying a target processor register capability" (column 6, lines 64-68 to column 7, lines 1-7; and column 7, lines 19-30). Thus, accordingly, this claim is also anticipated by Benson.

Per Claims 12-20:

These are method versions of the claimed device discussed above (claims 2-10, respectively), wherein all claim limitations also have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Benson.

Response to Arguments

6. Applicant's arguments with respect to claims 1-20 have been fully considered but they are not persuasive.

In the remarks, the applicant argues that:

a) The Office Action asserts that Benson discloses "a controller dividing the source code into translated code blocks of the target code based on a target processor register capability," as recited in claims 1 and 11. However, Applicants submit that Benson does not disclose such a controller.

The Examiner argued during the Interview, that it is not clear in claim 1, when the dividing is taking place in the process of translating the code. However, Applicants submit that the Examiner's position is moot, as Benson simply does not disclose, teach or even suggest "dividing the source code, based on a target processor capability."

In contrast to the subject matter recited in claim 1, Benson discloses dividing the source code into code blocks based on the occurrence of branches and loops in the source code (See for example col. 10, lines 26-29). As such, Benson does not disclose dividing the source code into code blocks based on the target processor capability. For example, when the source processor has 16 registers, and the target processor has only 8, Benson does not address how such a situation is handled. Benson does mention target processor capability, but merely discloses that a prologue and epilogue code are supplied for any routine which destroys the contents of a register.

The Office Action cites col. 4, lines 13-18 and col. 4, lines 67-68 - col. 5, lines 1-18 of Benson, which discloses that "The input code is parsed to determine its content, with the basic building blocks of the code identified (separated) and converted into an intermediate language.

The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine...In code generated by the compiler for register saves for an advanced 64-bit RISC architecture, only the low 32-bits of the 64-bit register can be put on the stack ...Accordingly, in one embodiment of the invention, the compiler tracks register usage to determine which registers are destroyed by a routine, and generate routine prologue and epilogue code which performs 64-bit register saves."

Benson is silent as to whether the structure or organization of these routines is based on target processor register capability, or whether the flow analyzer techniques are based on target processor register capability. Instead, Benson merely discloses that the compiler generates prologue and epilogue code which performs a 64-bit register save on registers which are determined to be destroyed by a routine. Benson does not disclose "dividing the source code ...based on the target processor register capability," as recited in claim 1.

Therefore, the subject matter recited in claim 1 is not anticipated by Benson. Therefore, Applicants respectfully request that the rejection of independent claim 1 and dependent claims 2-10 be withdrawn.

Examiner's response:

a) Examiner strongly disagrees with applicant's assertion that Benson fails to disclose the claimed limitations recited in claims 1-10. Benson clearly shows each and every limitation in claims 1-10. As previously pointed out in Paper nos. 3 and 4, Benson teaches a controller, the controller dividing the source code into translated code blocks of the target code based on a

target processor register capability (column 4, lines 3-18; and column 4, lines 67-68 to column 5, lines 1-18; the code translator divides the source code into basic blocks; when the code is converted from one architecture to another, the compiler tracks register usage). In addition, see the rejection above in paragraph 5 for rejections to claims 1-10.

In the remarks, the applicant argues that:

b) The Office Action rejects claims 11-20 under 35 U.S.C. §102(b) over Benson. However, claim 11 recites the same patentable feature as was recited in claim 1, which is "dividing the source code into translated code blocks of the target code based on the target processor register capability." Therefore, claim 11 recites patentable subject matter for similar reasons set forth above. Applicants respectfully request that the rejection of independent claim 11 and dependent claims 12-20 be withdrawn.

Examiner's response:

b) Examiner strongly disagrees with applicant's assertion that Benson fails to disclose the claimed limitations recited in claims 11-20. Benson clearly shows each and every limitation in claims 11-20. The Examiner has already addressed the applicant's arguments regarding claim 1 in the Examiner's Response (a) above. In addition, see the rejection above in paragraph 5 for rejections to claims 11-20.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

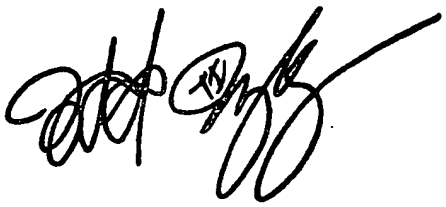
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication from the examiner should be directed to Qamrun Nahar whose telephone number is (703) 305-7699. The examiner can normally be reached on Mondays through Thursdays from 9:00 AM to 6:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone number for the organization where this application or processing is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

QN
August 12, 2003



Todd Ingberg
Primary Examiner
Group 2100